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10EC666

Sixth Semester B.E. Degree Examination, June/July 2018
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO full questions from each part.***

PART – A

1 a. Develop a sequential circuit that has a single data input signal, S and produces an output Y. The output is '1' whenever S has the same value over three successive clock cycles and '0' otherwise. Assume that the value of S for a given clock cycle is defined at the time of rising clock edge at the end of the clock cycle. **(05 Marks)**

b. Explain the following constraints imposed in real world circuits:
i) Wire delay
ii) Static load levels. **(10 Marks)**

c. Write short notes on Embedded Systems Design. **(05 Marks)**

2 a. Develop a test bench model for the light_controller_and_enable_module for the traffic light control. Verify the conditions that, when the enable input is '1', the output is same as the light input and when the enable input is '0', all light outputs are inactive. **(10 Marks)**

b. Design an encoder for use in a domestic burglar alarm that has sensors for each of eight zones. Each sensor signal is '1' when an intrusion is detected in that zone and '0' otherwise. The encoder has three bits of output, encoding the zones as follows:
zone 1 : 000 zone 2 : 001 zone 3 : 010 zone 4 : 011
zone 5 : 100 zone 6 : 101 zone 7 : 110 zone 8 : 111. **(10 Marks)**

3 a. Develop a verilog model of a code converter to convert the 4-bit, Gray code to a 4-bit unsigned Binary Integer. **(05 Marks)**

b. Develop a verification test bench for the adder/subtractor that compares the result with the result of addition or subtraction performed on values of type integer. **(10 Marks)**

c. Develop a verilog model of a 4 to 1 multiplexer that selects among four unsigned 6-bit integers. **(05 Marks)**

4 a. Develop a verilog model for an interval timer that has clock, load and data i/p ports and a terminal-count output port. The timer may be able to count intervals upto 1000 clock cycles. **(04 Marks)**

b. Develop a verilog model of the complex multiplier datapath. **(06 Marks)**

c. Design a circuit that counts 16 clock cycles and produces a control signal, "Ctrl", that is '1' during every eighth and twelfth cycle. Also develop a verilog model for the same. **(10 Marks)**

PART – B

5 a. Write about Field Programmable Gate Arrays. **(10 Marks)**

b. Design a 64k × 8 bit composite memory using four 16k × 8 bit components. **(10 Marks)**

6 a. Explain in detail the following Gumnut instruction set:
   i) Arithmetic and logical instructions
   ii) Memory and I/O instructions
   iii) Branch instructions
   iv) Shift instructions
   v) Jump instructions. **(10 Marks)**

   b. Sketch the little-endian and big-endian memory layout for data words. **(04 Marks)**

   c. Write short notes on cache memory. **(06 Marks)**

7 a. Explain the following parallel buses:
   i) Multiplexed buses
   ii) Open-drain buses. **(10 Marks)**

   b. Explain in detail the three basic ways in which we can synchronize the transmitter and receiver. **(10 Marks)**

8 a. Suppose the execution time is estimated for the various parts of an algorithm on an embedded processor. The algorithm has two Kernels, one that consumes 80% of the execution time and another that consumes 15% using a hardware accelerator, we could speed up execution of the first Kernel by a factor of 10 or the second by a factor 100, which accelerator gives the best overall performance improvement? **(05 Marks)**

   b. Explain in detail Boundary Scan Technique. **(10 Marks)**

   c. Explain the concept of fault models and fault simulation to detect a fault within a circuit. **(05 Marks)**

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